**NorthSouthUniversity**

Department of Computer Science and Engineering

**Final,**Spring-2017

Course No: **CSE231** Course Title: **Digital Logic Design**

Time:1 h 10 min Full Marks:30

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| 1. | Consider the following sequential circuit that has two flip-flops A and B and one input x. It consists of a combinatorial logic connected to the D flip-flops, as shown in Figure below. Analyze the circuit:  a) Derive the next state and output equations.  b) Derive the state table of the sequential circuit.  c) Draw the corresponding state diagram. | 12 |
| 2. | a. Design a 3 bit ring counter | 3 |
|  | b. Design a 3 bit serial to parallel data converter. It takes 3 bit data in serial and outputs them in parallel.  . | 5 |
| 3. | Design a 4x4 ROM with the following contents.   |  |  | | --- | --- | | Address | Data | | 000 | 0001 | | 001 | 0010 | | 010 | 1100 | | 011 | 0010 | | 3 |
| 4. | a. Design a 3 bit counter that counts the number in the form of power of 2. You have to provide the state diagram | 3 |
|  | b. Now consider that, the counter you designed previously is connected with another circuit. The purpose of this circuit is to detect the value of powerfrom the counter output. Design the circuit.  Detect the power from the counter output  Counter  (Outputs the value of power of 2)  power | 4 |
| 5. | (Bonus) You designed a ROM in question 3. Now designanew circuitthat will detect whether a ROM output is even or odd. If the content of the ROM is even it will display 1, if odd it will show 0.  **Block diagram (with sample input)**  The following diagram shows that if the we input 000 in address line the content of ROM is 001, which will be the inputfor the new circuit. Since 001 is odd number, the new circuit will output 0.  0  0001  00  (new circuit)  Detect even or odd  4x4  ROM | 5 |